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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/595,168	03/16/2006	Atsushi Tabuchi	CNP-US030140	3831

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EXAMINER	
SHAH, TUSHAR S	
ART UNIT	**PAPER NUMBER**
2184	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/595,168	TABUCHI, ATSUSHI	
	Examiner	Art Unit	
	Tushar S. Shah	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/21/2006;6/11/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the application filed on March 16th, 2006.

Status of Claims

Claims 1-7 have been presented for examination. Claim 1 is in independent form. Claims 1-7 are rejected under U.S.C. 103(a).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiga US Patent No. 5,781,599 (hereinafter Shiga) in view of Lowe et al. US Patent No. 6,300,985 (hereinafter Lowe).

Referring to claim 1, Shiga discloses, a data conversion system wherein one of first and second nodes on an IEEE1394 bus serves as a cycle master (on a IEEE 1394

bus one device serves as a cycle master, Shiga column 1, lines 30-40), first data (MPEG transport stream, Shiga column 3, lines 18-19) is transferred from the first node to the second node (the stream is transported across the P1394 bus, Shiga column 3, lines 18-19) in synchronism with a cycle start packet output from the cycle master (in the first packet of data transmitted, a cycle start packet is included to synchronize the decoder, Shiga column 3, lines 12-20).

Shiga also discloses, a synchronization adjustment unit (cycle timer, Shiga column 4, lines 36-39) for synchronizing the frequency of the cycle start packet output from the cycle master with the frequency of the reference signal received by the external synchronizing signal receiver (the cycle timer utilizes the sync time included periodically within incoming packets to adjust for the lag between the source and the receiver, Shiga column 44, lines 40-47).

It is noted however that Shiga does not disclose, second data generated by conversion of the first data in the second node is synchronized with an external reference signal and output.

Lowe on the other hand, achieves the claimed feature, second data (serial digital interface output (SDI), Lowe column 2, lines 1-2) generated by conversion of the first data in the second node is synchronized with an external reference signal (Reference Input, Lowe Fig. 1) and output (The SDI signal is output from block 14, Lowe column 3, lines 34-37 and Fig. 1).

It is noted that Shiga also does not disclose, an external synchronizing signal receiver for receiving an external reference signal provided on at least one of the first and second nodes.

On the other hand, Lowe achieves the claimed feature, an external synchronizing signal receiver (video processor 10, Lowe column 3, lines 24-25 and Fig. 1) for receiving an external reference signal provided on at least one of the first and second nodes.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Shiga to output to SDI rather than NTSC and to synchronize it with an external reference input. Shiga in fact, already converts the incoming MPEG data to a serial bit stream in block 10 of figure 6. Shiga takes this digital stream and decodes it to be converted to NTSC. The motivation to combine is apparent in Lowe, specifically column 1, lines 25-36, where it states that with the transition to digital television it is necessary to utilize a conversion to SDI because the prior standards, such as NTSC and PAL, produce flawed images in digital television sets.

As per claim 2, Shiga discloses, the data conversion system according to claim 1, wherein the first node (anyone of CAM1, or VTR 1-3, the receiving and transmitting capabilities are provided in each device, Shiga column 5, lines 51-54) is hardware comprising a 1394OHCI compliant IEEE1394 interface (P1394 interface receives data

from the P1394 serial bus 1, Shiga column 5, lines 57-59) for outputting a video signal in DV format as first data (MPEG transport stream column 3, lines 18-19),

It is noted however that Shiga does not disclose, the second node is data conversion hardware for outputting an analog video signal or SDI video signal as second data.

On the other hand, Lowe achieves the claimed feature of, the second node is data conversion hardware (conversion of parallel digital signals into a serial digital signal, Lowe column 1, lines 50-51) for outputting an analog video signal or SDI video signal as second data (The SDI signal is output from block 14, Lowe column 3, lines 34-37 and Fig. 1).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Shiga to output to SDI rather than NTSC. Shiga in fact, already converts the incoming MPEG data to a serial bit stream in block 10 of figure 6. Shiga takes this digital stream and decodes it to be converted to NTSC. The motivation to combine is apparent in Lowe, specifically column 1, lines 25-36, where it states that with the transition to digital television it is necessary to utilize a conversion to SDI because the prior standards, such as NTSC and PAL, produce flawed images in digital television sets.

As per claim 3, Shiga further discloses, the data conversion system according to claim 1, wherein the second node comprises the synchronization adjustment unit (cycle timer is included in every piece of equipment as in fig 1, Shiga column 4, lines 36-39),

and serves as cycle master for data transfer (inherent, any device may serve as the cycle master on the IEEE 1394 bus, Shiga column 1, lines 30-40).

It is noted however that Shiga does not disclose, wherein the second node comprises the external synchronizing signal receiver.

On the other hand, Lowe achieves the claimed feature, wherein the second node comprises the external synchronizing signal receiver (Reference Input, Lowe Fig. 1).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Shiga to output to SDI rather than NTSC. Shiga in fact, already converts the incoming MPEG data to a serial bit stream in block 10 of figure 6. Shiga takes this digital stream and decodes it to be converted to NTSC. The motivation to combine is apparent in Lowe, specifically column 1, lines 25-36, where it states that with the transition to digital television it is necessary to utilize a conversion to SDI because the prior standards, such as NTSC and PAL, produce flawed images in digital television sets.

As per claim 4, Shiga discloses, the data conversion system according to claim 1, wherein the first node comprises the synchronization adjustment unit, the second node comprises the external synchronizing signal receiver and synchronization adjustment unit (all the equipment in Shiga contains the cycle timer circuits, Shiga column 4, lines 36-39), and the cycle start packet frequency is synchronized with the frequency of the reference signal received by the external synchronizing signal receiver by means of the synchronization adjustment unit of the node that serves as cycle

master (the cycle timer utilizes the sync time included periodically within incoming packets to adjust for the lag between the source and the receiver, Shiga column 44, lines 40-47).

As per claim 5, Shiga further discloses the data conversion system according to claim 4, wherein when the first node serves as cycle master (inherent, any device may serve as the cycle master on the IEEE 1394 bus, Shiga column 1, lines 30-40), the reference signal received by the external synchronizing signal receiver of the second node is transmitted from the second node to the first node by asynchronous transfer of the IEEE1394 interface (the reference signal is extracted from packets sent across the PIEE1394 bus, Shiga column 4, lines 30-39).

As per claim 6, Shiga further discloses, the data conversion system according to claim 4, comprising a dedicated synchronization signal line (the reference signal is used to calculate position information for the decoder to match clock signals, column 2, lines 57-62) for transmitting the reference signal received by the external synchronizing signal receiver of the second node from the second node to the first node when the first node serves as cycle master (inherent, any device may serve as the cycle master on the IEEE 1394 bus, Shiga column 1, lines 30-40).

As per claim 7, Shiga discloses the data conversion system according to claim 1, wherein the first node comprises the external synchronizing signal receiver and

synchronization adjustment unit (all the equipment in Shiga contains the cycle timer circuits and equivalent circuits, Shiga column 4, lines 36-39), and serves as cycle master for data transfer (inherent, any device may serve as the cycle master on the IEEE 1394 bus, Shiga column 1, lines 30-40).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Eyer US Publication No. 2002/0049879 A1 discloses a combined IEEE 1394 and DVI cable and connections.

Sato US Patent No. 6,128,318 discloses a method for synchronizing a cycle master and slave node using an external reference.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tushar S. Shah whose telephone number is (571)-270-1970. The examiner can normally be reached on Mon-Fri 7:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on 571-272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

T.S.

HENRY TSAI
SUPERVISORY PATENT EXAMINER

1/22/08